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OPTOELECTRONIC TECHNOLOGY CONSORTIUM

Quarterly Technical Report No. 6
October 1 to December 31, 1993
Honeywell, Inc.

1.0 Introduction.

The Optoelectronic Technology Consortium has been established to position U.S. industry as the world leader in optical interconnect technology by developing, fabricating, integrating and demonstrating the producibility of optoelectronic components for high-density/high-data-rate processors and accelerating the insertion of this technology into military and commercial applications. This objective will be accomplished by a program focussed in three areas.

Demonstrated performance: OETC will demonstrate an aggregate data transfer rate of 16 Gb/s between single transmitter and receiver packages, as well as the expandability of this technology by combining four links in parallel to achieve a 64 Gb/s link.

Accelerated development: By collaborating during the precompetitive technology development stage, OETC will advance the development of optical components and produce links for a multiboard processor testbed demonstration.

Producibility: OETC's technology will achieve this performance by using components that are affordable, and reliable, with a line BER<10^{-15} and MTTF>10^{6} hours.

Under the OETC program Honeywell will develop packaged AlGaAs arrays of waveguide modulators and polymer based, high density, parallel optical backplane technology compatible with low-cost manufacturability.

The packaged AlGaAs modulator arrays will consist of a single fiber input, a 1x4 fanout circuit, four waveguide modulators, and four fiber outputs, all mounted on a ceramic header. The primary benefits to this approach are enhanced system reliability, particularly at high temperatures, and a device design that is highly producible due to the inherent process tolerance. Combined with the demonstrated high density of these devices when fabricated in arrays, this allows the development of compact and reliable transmitter components.

The objective of the polyimide backplane development effort is to demonstrate a practical high density (>20 lines or channels per mm) parallel optical backplane facilitating (bandwidth x length/power) interconnect figures of merit between one and two orders of magnitude greater than would be attainable with state-of-the-art electrical interconnects.

The effort will address both development of an ultimately manufacturable and environmentally tolerant optical backplane, and the optical interface concepts required for practical board-to-backplane optical connection. The key functionalities, and compatibility with standard multiboard assembly practices will be demonstrated in a laboratory evaluation system.

Technical progress achieved during the current reporting period, and plans for the next reporting period, are summarized in the following sections.

2.0 Progress Summary.

2.1 AlGaAs Modulator Array Development. Task leader: Dr. Mary Hibbs-Brenner

During the previous reporting period, a mask set was developed which is expected to produce the devices which are deliverables under the program. The mask set allows the fabrication of modulator arrays with four Mach-Zehnder modulators per array, and the appropriate bond pads which allow the devices to be packaged together with the modulator drivers chips designed by Martin Marietta. This mask set was used to fabricate a first pass of the final configuration, also during the previous reporting period. Arrays suitable for packaging and delivery were produced. However, the presence of an oxide passivating layer was found to somewhat degrade the achievable contrast ratio of the devices, and also reduced the performance as a function of temperature. We believe the observed degradation of performance to be due to additional stress induced by the oxide layer.

During the current reporting period, a second process run was carried out, with the process modified slightly to eliminate the oxide passivation. Improved performance at both room temperature and high temperatures was observed.

The performance of the best array from the current process run is compared in Figure 1 to the performance of the best array from the process run completed in the previous quarter. Contrast ratio, maximum optical power output, V-pi, and bias voltage are plotted as a function of the modulator arm number in the array for both arrays. Although a single sided drive was provided for device testing, a complementary drive scheme will be used in the package. Sample 212C L3-5 is the new array processed this quarter, which had 5mm long electrodes. The array also incorporated a splitter which was 30um longer than the design calculated to be the baseline. Since the sample it is compared to, 213D, had 3mm long electrodes, the drive voltage is normalized by using the voltage length product. It can be seen that the voltage-length product (Figure 1(a)) is very similar for both arrays, and very uniform across an array. The drive voltage for Sample 212C would be just under 5 volts, or +/- 2.5V, while the effective drive voltage for sample 213D would be around 8 volts, or +/- 4 volts. On the other hand, the bias voltage (Figure 1(b)) is not as uniform, which will necessitate tailoring a separate bias voltage for each modulator in the array. This has already been accounted for in the package which has been designed. The

difference in the magnitude of the required bias voltage between 212C and 213D is also due to the different electrode lengths. Improvement over the previous quarter's results is seen in contrast ratio (Figure 1(c)). The lowest contrast arm in array 212C is 9.9dB, whereas the contrast ratio dips as low as 6dB for array 213D. The maximum power output also appears significantly higher in Sample 212C (Figure 1(d)). However, this is dependent on the coupling efficiency into the unpackaged end-face during testing, which is a value which may vary from day to day, and is very difficult to quantify. Therefore it is premature to conclude that insertion loss is significantly lower in this sample.

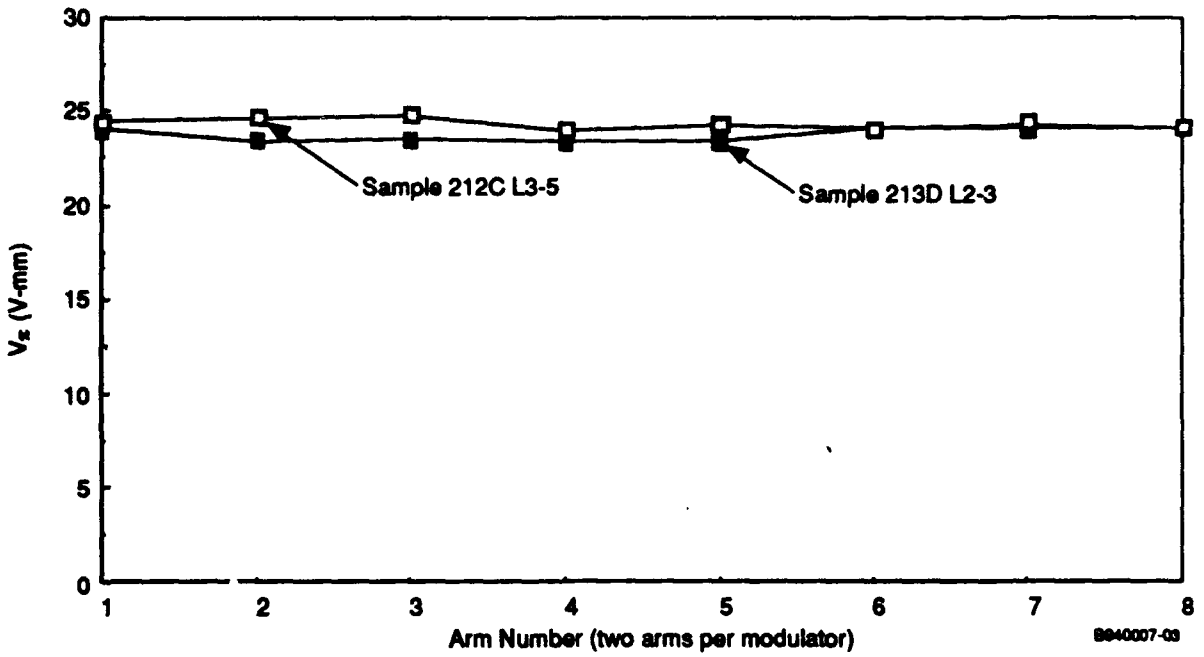
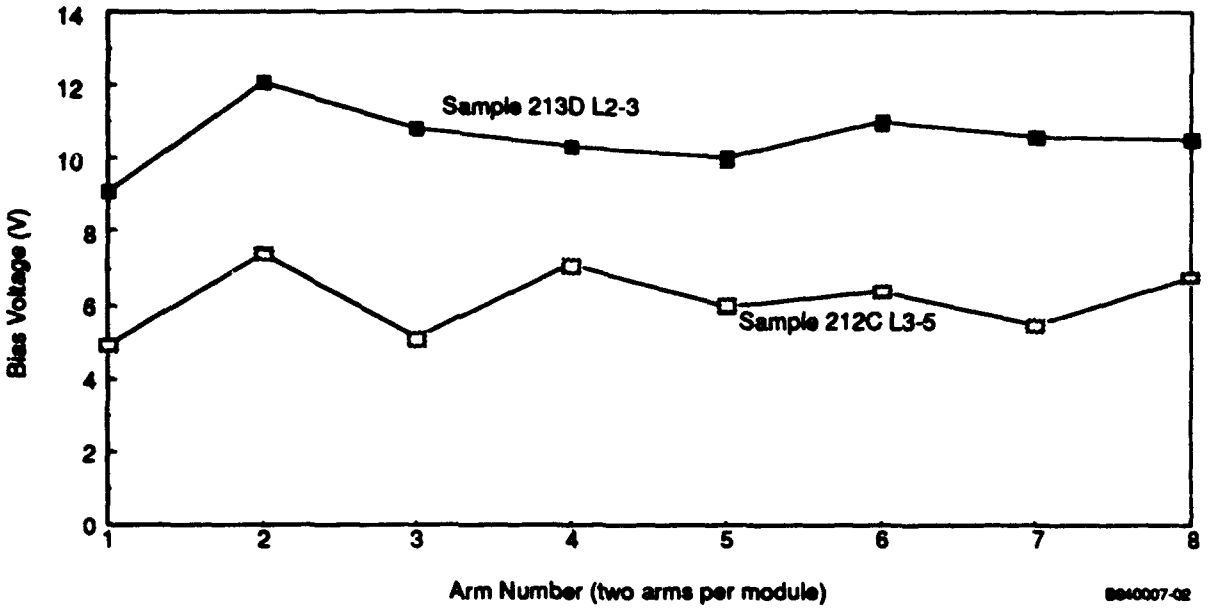
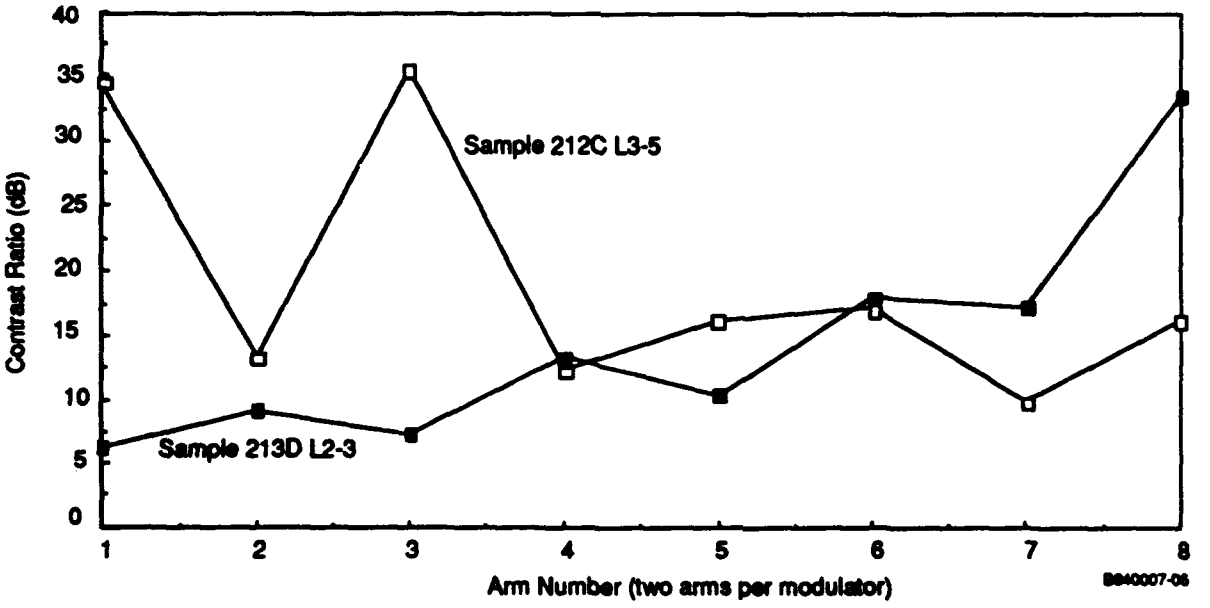


Figure 1. Comparison of performance from the recent fabrication run (212C) to the previous fabrication run.

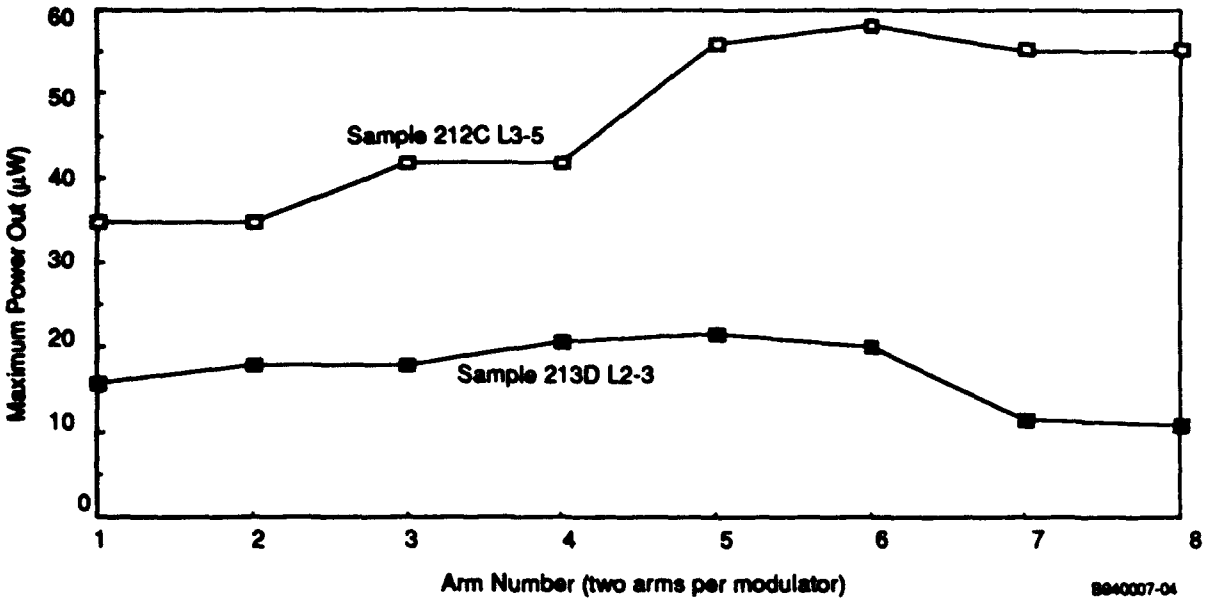
(a) Voltage-length product (V_π) versus modulator arm number.



(b) Bias voltage.



(c) Contrast ratio.



(d) Maximum Optical Power Output

Performance as a function of temperature was also measured on a device from sample 213C. 213C comes from the same OMVPE wafer growth as 213D, but was processed in the most recent fabrication run. The sample was tested up to 136 C, and the results are displayed in Figure 2. The performance over this temperature range is significantly improved when compared to the previous quarter's results on sample 213D. In the region closest to 0 volts, which is where the packaged device will be operated, there is less than 1dB degradation in either optical throughput power and contrast ratio remains greater than 10 dB. We believe the improved performance is due to the elimination of the oxide passivating layer.

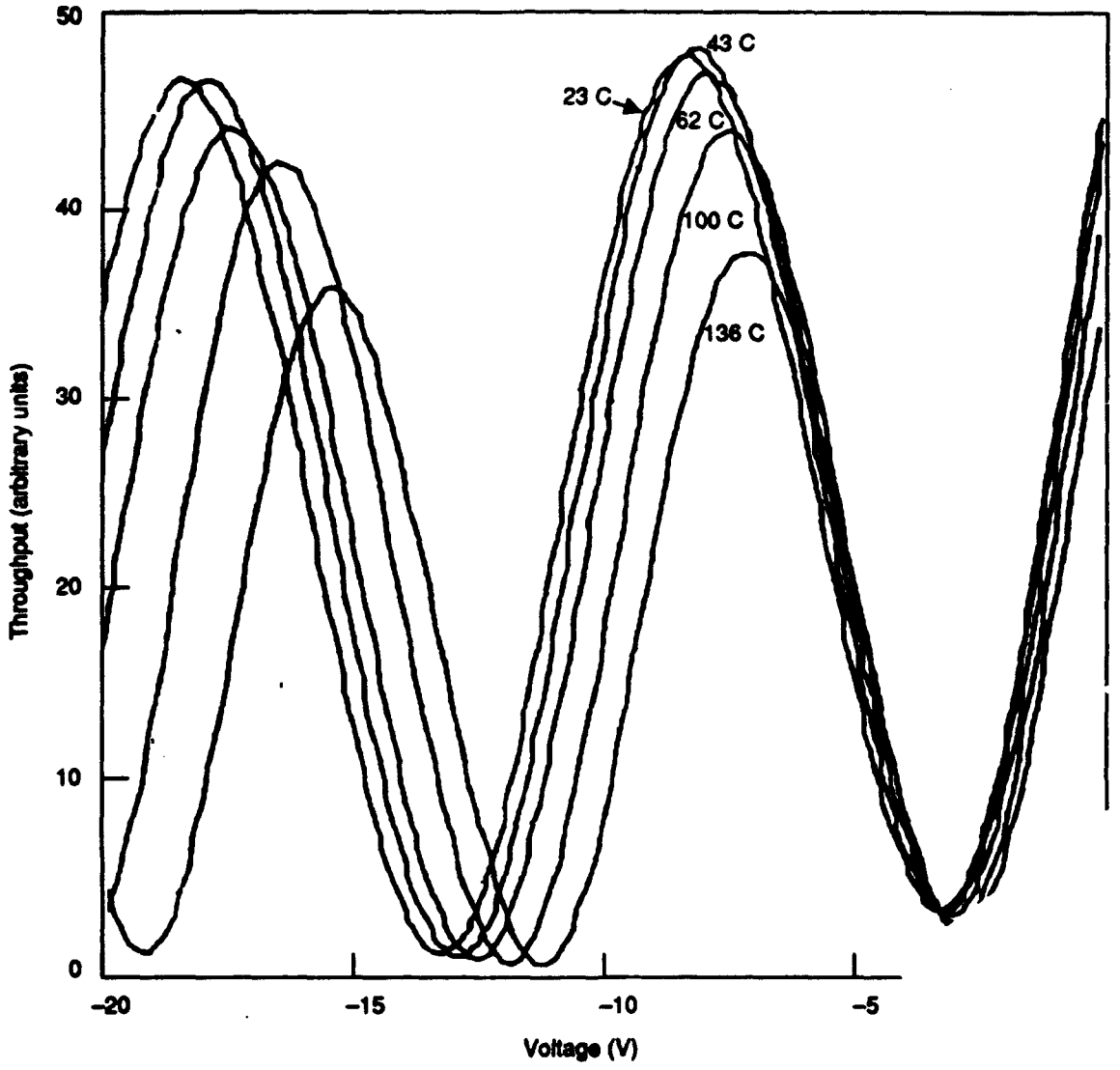


Figure 2. Light versus applied voltage (L-I) curves as a function of sample temperature. Device is tested with a single-sided drive.

Effort this quarter also included the design and fabrication of a test fixture which will allow us to measure the frequency response of the waveguide modulators. While the package being developed under the packaging task will in principle allow operation of the modulator arrays at the speeds required for the links, it is important to evaluate the frequency response of the individual chips in order to be able to troubleshoot should problems arise in achieving high frequency performance. The test fixture basically translates between coplanar probes and the bond pads provided on the modulator array chip.

2.2 AlGaAs Modulator Array Packaging. Task leader: Mr. John Lehman

During the current reporting period a complete modulator array module was assembled, including (non-functional) modulator array and driver chips. Although the chips were intentionally non-functional, the exercise provided useful feedback on the feasibility of the physical layout, and as a result two design changes will be made. The first change is a result of insufficient package height to accomodate the height of the alumina v-block (which holds the single-mode PM fiber for alignment) which is simply corrected by adding one more layer of alumina to the leadframe. The second change deals with the arrangement of the de-coupling capacitors for the modulator driver voltage supply. The original placement made bonding difficult. However, the placement is easily modified to facilitate bonding. A photograph of the assembled modulator package is shown in Figure 3.

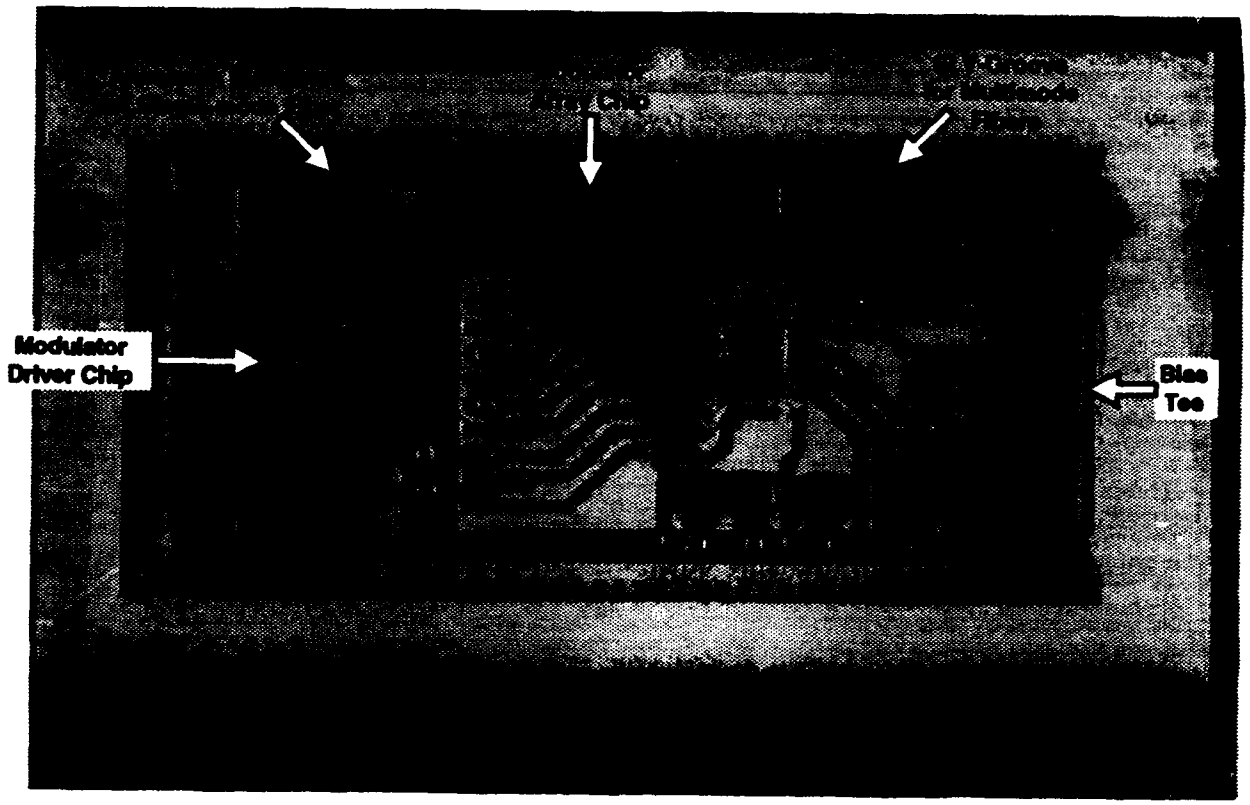


Figure 3. Photograph of the assembled modulator array package.

2.3. Polymer Backplane Development. Task leader: Dr. Julian Bristow

During this reporting period, data related to the excess loss of waveguide bends as a function of the radius of curvature was acquired. Although the samples were prepared and tested under another program (Optical Interconnect Technology, or OIT, funded by ARPA), knowledge of the radius of curvature which gives the minimum insertion loss was necessary input for the design of the masks to be used to pattern the polymer waveguides for the final demonstration under this task. Since the results depend upon the particular polymers chosen for the core and cladding layers, this data could only be gathered after the choice of optimum materials was finalized. Bends with radii of curvature ranging from 0.5mm to 10mm were measured. Although there was a fair amount of scatter in the data, the best results were achieved for 4 to 6mm bend radii, where the excess insertion loss ranged between 0.1 and 0.7dB. This data will now be used to design the mask used to pattern the board and backplane polymer waveguides for the demonstration.

3.0. Next quarter plans.

3.1. AlGaAs Modulator Array Development.

Testing will continue on modulator arrays from the most recent fabrication run. Testing will include evaluation of contrast ratio, optical throughput, and required drive and bias voltages. Performance over a range of temperatures will be carried out. In addition, high speed testing of the modulator arrays will be carried out up to modulation rates of at least 3 GHz using the test fixture which has been fabricated during the current reporting period. If necessary, an additional fabrication run will be executed in order to provide sufficient modulator arrays for packaging.

3.2. AlGaAs Modulator Array Packaging.

The modifications to the package mentioned above will be carried out and we will begin assembling complete packages, using functional modulator array and driver chips. Testing of packaged devices will then include measurement of fiber to fiber insertion loss, modulation contrast ratio, array uniformity, high frequency characteristics, and performance over a range of temperatures.

3.3. Polymer Backplane Development.

During the next quarter the mask design for the polymer waveguides on the board and backplane will be finalized and masks fabricated. Boards with polymer waveguides will then be fabricated, and connector fixtures will be attached. The demonstration to be carried out will include the propagation of a signal from transmitter into the board waveguide, through a connector into the backplane waveguide (which includes both a bend and a splitter), through another connector back into another board waveguide, and finally

into a receiver. We shall assess the connector loss, alignment tolerance, and system bit error rate.

4.0. Summary.

During the current quarter, additional modulator arrays suitable for packaging as deliverables have been fabricated and tested. Improvements in performance at room and elevated temperatures have been demonstrated. A test fixture allowing high frequency performance of unpackaged modulator arrays has been designed and fabricated. Testing at a range of frequencies and temperatures will continue on into next quarter. Additional modulator arrays will be fabricated, if necessary.

A first pass at assembling a package has been carried out, using non-functional chips. Some minor layout problems and their solutions have been identified. Packaging of functional arrays and driver chips will be performed next quarter. The performance of the fully packaged devices will be evaluated.

The last piece of data required for the design of the mask for the polymer waveguide for the demonstration was acquired, and mask design begun. During the next quarter the polymer waveguides on the boards will be fabricated and the demonstration will be assembled and evaluated.